



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,066	07/08/2003	Kenta Kato	024016-00064	7503

4372 7590 02/22/2005

ARENT FOX KINTNER PLOTKIN & KAHN
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER

MAI, SON LUU

ART UNIT PAPER NUMBER

2827

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/614,066

Applicant(s)

KATO, KENTA

Examiner

Son L. Mai

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 4 and 16-18 is/are rejected.
- 7) ☒ Claim(s) 2 and 5-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 07-08-03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed 07-08-03 has been considered.

Specification

3. The disclosure is objected to because of the following informalities:
On page 12, line 28, the reference character "RCV" should be --RC--.
On page 17, line 2, "establish" should read -- established--.
4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 4, 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,370,060 issued to Takata et al. (hereinafter Takata).

Regarding claim 1, Takata discloses a semiconductor memory device that differentially amplifies data readout from a memory cell with reference to a reference value when data is read out (SA performs this function.) The semiconductor memory

Art Unit: 2827

device comprises: a reference cell (T_{ref} in figure 1); and a load adjustor section (190) that adjusts a first load connected to the reference cell in accordance with a selected address (bank select signal B_{sa}) of the memory cell; wherein the first load is adjusted with reference to a second load on a data path of the memory cell selected in accordance with the selected address (column 10, lines 51-57).

Regarding claim 3, Takata teaches at column 10, line 58 through column 11, line 3, that the first load is equivalent to the second load.

Regarding claim 4, Takata also teaches the load adjustor section (190) comprising a load element group that includes a plurality of load elements (Cr_0 - Cr_m), and a selector section (Lt_0 - Lt_m) that selects predetermined at least one of the load elements as the first load from the load element group by the selected address.

Regarding claim 16, Takata discloses that the semiconductor memory device is a non-volatile semiconductor memory device (column 1, lines 5-10), and the reference value is a reference current value (reference voltage at node Br also carries a current.)

Regarding claim 17, Takata discloses a control method of a semiconductor memory device comprising the steps of: a step for reading out data from a memory cell (column 11, lines 27-44), and a step for differentially amplifying the data read out from the memory cell with reference to a reference value read out from a reference cell (column 12, lines 22-38); wherein the reference value is adjusted by adjusting a first load (190) connected to the reference cell with reference to a second load on a data path of the memory cell selected by a selected address (column 10, line 51 through column 11, line 3).

Regarding claim 18, Takata teaches at column 10, line 58 through column 11, line 3, that the first load is equivalent to the second load.

Allowable Subject Matter

7. Claims 2, 5-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach at least the limitation of the second load is a load at a source terminal side of the memory cell according to the selected address, and the load adjustor section is arranged at a source terminal side of the reference cell.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Akaogi (U.S. Patent 5,091,888) and Wu et al. (U.S. Patent 6,754,106) teach reference memory cells having adjusting sections to accommodate loading effects of bit lines.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

02-15-05



Son L. Mai
Primary Examiner
Art Unit 2827

